Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.–13. (Canceled)

14. (Currently Amended) A semiconductor structure, comprising:

a semiconductor substrate;

a well implanted in the substrate, the well having an opposite conductivity type with respect to the substrate;

first and second dielectric spacers positioned on the substrate and defining opposite sides of an opening;

a gate dielectric positioned on the substrate and in the opening;

a gate electrode formed in the opening and on the gate dielectric, the gate electrode being limited by the dielectric spacers;

first and second halos implanted in the well and under the first and second dielectric spacers, respectively, a channel being defined in the well by the halos; ~~and~~

source and drain regions implanted in the substrate and adjacent to the first and second halos, respectively;

a first contact coupled to a first one of the source and drain regions and positioned on a first portion of the gate electrode;

a second contact coupled to a second one of the source and drain regions; and

a dielectric layer positioned on a second portion of the gate electrode and being defined on opposite sides by the first and second contacts.

15. (Original) The semiconductor structure of claim 14, further comprising dielectric isolation structures formed in the substrate on opposite sides of the well.

16. (Original) The semiconductor structure of claim 14 wherein the first and second halos are formed by ion implanting at plural angles through the opening prior to forming the gate electrode in the opening, the plural angles being sufficient to form the halos only under the dielectric spacers without extending directly under the opening.

17. (Original) The semiconductor structure of claim 14 wherein the dielectric spacers have a height that is more than twice a width of the spacers.

18. (Original) The semiconductor structure of claim 14, further comprising silicide contacts formed on the gate electrode, source, and drain.

19. (Canceled)

20. (New) A semiconductor structure, comprising:

a semiconductor substrate;

first and second dielectric spacers positioned on the substrate and defining opposite sides of an opening;

a gate dielectric positioned on the substrate and in the opening;

a gate electrode formed in the opening and on the gate dielectric, the gate electrode being limited by the dielectric spacers;

source and drain regions implanted in the substrate and adjacent to a channel region underlying the gate dielectric;

a first contact coupled to a first one of the source and drain regions and positioned on a first portion of the gate electrode;

a second contact coupled to a second one of the source and drain regions; and

a dielectric layer positioned on a second portion of the gate electrode and being defined on opposite sides by the first and second contacts.

21. (New) The semiconductor structure of claim 20, further comprising a well implanted in the substrate, the well having an opposite conductivity type with respect to the substrate.

22. (New) The semiconductor structure of claim 21, further comprising dielectric isolation structures formed in the substrate on opposite sides of the well.

23. (New) The semiconductor structure of claim 20, further comprising first and second halos implanted in the substrate and under the first and second dielectric spacers, respectively, the channel being defined in the substrate by the halos.

24. (New) The semiconductor structure of claim 23 wherein the first and second halos are formed by ion implanting at plural angles through the opening prior to forming the gate electrode in the opening, the plural angles being sufficient to form the halos only under the dielectric spacers without extending directly under the opening.

25. (New) The semiconductor structure of claim 20 wherein the dielectric spacers have a height that is more than twice a width of the spacers.

26. (New) The semiconductor structure of claim 20, further comprising silicide contacts formed on the gate electrode, source, and drain, the silicide contacts formed on the gate electrode and the first one of the source and drain regions being positioned under the first contact and the silicide contact formed on the second one of the source and drain regions being positioned under the second contact.

27. (New) A semiconductor structure, comprising:

a semiconductor substrate;

a gate dielectric positioned on the substrate;

a gate electrode positioned on the gate dielectric;

first and second dielectric spacers positioned on the substrate and defining opposite sides of the gate electrode;

source and drain regions implanted in the substrate and adjacent to a channel region underlying the gate dielectric;

a first contact coupled to a first one of the source and drain regions and positioned on a first portion of the gate electrode;

a second contact coupled to a second one of the source and drain regions; and

a dielectric layer positioned on a second portion of the gate electrode and being defined on opposite sides by the first and second contacts.

28. (New) The semiconductor structure of claim 27, further comprising a well implanted in the substrate, the well having an opposite conductivity type with respect to the substrate.

29. (New) The semiconductor structure of claim 28, further comprising dielectric isolation structures formed in the substrate on opposite sides of the well.

30. (New) The semiconductor structure of claim 27, further comprising first and second halos implanted in the substrate and under the first and second dielectric spacers, respectively, the channel being defined in the substrate by the halos.

31. (New) The semiconductor structure of claim 30 wherein the first and second halos are formed by ion implanting at plural angles through the opening prior to forming the gate electrode in the opening, the plural angles being sufficient to form the halos only under the dielectric spacers without extending directly under the opening.

32. (New) The semiconductor structure of claim 27 wherein the dielectric spacers have a height that is more than twice a width of the spacers.

33. (New) The semiconductor structure of claim 27, further comprising silicide contacts formed on the gate electrode, source, and drain, the silicide contacts formed on the gate electrode and the first one of the source and drain regions being positioned under the first contact and the silicide contact formed on the second one of the source and drain regions being positioned under the second contact.